1. A method for controlling and driving external higher voltage switching devices, such as transistors, thyristors or triacs e.g. which are configured as a half-bridge circuit branch, i.e. forming an output voltage terminal as mid-point between a high-side and a low-side switching device, both connected in series between a main supply voltage terminal, furnishing the main supply energy and a ground terminal respectively, comprising:

providing said main supply voltage terminal, said output voltage terminal, said ground terminal, said low-side switching device, said high-side switching device, an integrated low-side controller circuit, an integrated high-side controller circuit and both circuits containing four internal switches arranged as two pairs, means for transmitting/receiving said information data, means for transferring information, means for potential separation and isolation, storage means for said main supply energy, a first storage means for low-side auxiliary supply energy, a second storage means for high-side auxiliary supply energy;

arranging said external low-side switching device and said external high-side switching device in serial connection between said given power or high-side terminal and said ground or low-side terminal of the circuit, used for feeding input of said available main supply energy, thus creating said mid-point terminal for said output voltage between said two respectively attached high-side and low-side external switching devices;

associating to said external low-side switching device said integrated low-side controller circuit together with an individually controlled and

regulated low-side appliance for its required low-side auxiliary energy supply as said;

associating to said external high-side switching device said integrated high-side controller circuit together with an individually controlled and regulated high-side appliance for its required high-side auxiliary energy supply as said;

assigning said main supply energy to said storage means, placed between and connected to said integrated low-side controller circuit and said integrated high-side controller circuit;

assigning said low-side auxiliary supply energy to said first storage means, connected to said integrated low-side controller circuit;

assigning said high-side auxiliary supply energy to said second storage means, connected to said integrated high-side controller circuit;

collocating for the transporting and controlling of said main energy as well as said individually regulated low-side and high-side auxiliary supply energies said two pairs of internal low-side and high-side switches, internal to said integrated low-side and high-side controller circuits;

collocating for the generating, processing, and storing said information data said integrated low-side and said integrated high-side controller circuits for the purpose of control and regulation of each of said supply energies;

collocating for the transferring and/or exchanging of said information data with said isolating internal potential separation said means for

transferring information between said low-side controller circuit and said high-side controller circuit;

starting-up an initial bootstrap procedure for controlling and regulating said available main supply energy with said external switching devices; together with

generating said low-side and high-side auxiliary supply energies for said low-side controller and said high-side controller circuits;

generating, processing, and storing said information data, within said two integrated low-side and high-side controller circuits for the purpose of transportation, control and regulation of said main supply energy and said first and said second auxiliary supply energies in order to solve the required control task;

setting-up and following a four segment time slot scheme;

realizing said controlling of said four internal low-side and high-side switches with the help of said low-side and high-side controller circuits;

implementing said driving of said low-side and high-side controller circuits using said generated information data within the rules of said time slot scheme;

preparing transfer and/or exchange of said information data by transmitting/receiving said information data with said means for transferring information within and between said integrated low-side and high-side controller circuits;

preparing said means for transmitting/receiving said information data as said means for transferring information within said integrated low-side controller circuit;

preparing said means for receiving/transmitting said information data as said means for transferring information within said integrated high-side controller circuit;

setting-up the controlling and driving of said external low-side and said external high-side switching devices with the help of said low-side and said high-side controller circuits using said information data;

controlling and driving said low-side switching device with the help of said integrated low-side controller circuit;

controlling and driving said high-side switching device with the help of said integrated high-side controller circuit;

transferring and/or exchanging said information data between said integrated low-side and said integrated high-side controller circuits with said means for transferring information;

transmitting/receiving said information data with said means for transferring information at said integrated low-side controller circuit;

receiving/transmitting said information data with said means for transferring information at said integrated high-side controller circuit;

transporting and storing said energies between and in said storage devices with the help of said four internal switches; and at the same time

controlling and regulating said stored auxiliary supply energies within the framework of said time slot scheme;

transporting during the first time segment of said time slot scheme a controlled amount of said main supply energy into said means for storing said main supply energy and into said means for storing said low-side auxiliary supply energy;

storing said controlled amount of said main supply energy into said storage means for said main supply energy;

storing said controlled amount of said low-side auxiliary supply energy for said integrated low-side controller circuit into said first storage means;

transporting during the second time segment of said time slot scheme a controlled amount from said stored main supply energy into said means for storing said high-side auxiliary supply energy;

storing said controlled amount of said high-side auxiliary supply energy for said integrated high-side controller circuit into said second storage means;

transporting during the third time segment of said time slot scheme a controlled amount of said main supply energy into said means for storing said main supply energy;

storing said controlled amount of main supply energy into said storage means for said main supply energy;

transporting during the fourth time segment of said time slot scheme a controlled amount of said main supply energy to ground, thus reducing said main supply energy;

keeping the remainder of said main supply energy stored in said storage means for said main supply energy; and

controlling of said stored low-side and said stored high-side auxiliary supply energies by regulating its voltages according to the boundary conditions to be kept for the required control solution;

controlling of said output voltage at said mid-point terminal by regulating its behavior in such a way, that the required control task for the circuit is properly solved;

closing the operation loop by getting back to the first step after said initial bootstrap procedure; and

repeating this loop action permanently during the regular operation of the circuit.

2. The method according to claim **1** wherein said low-side controller circuit is being operated as master controller and said high-side controller circuit is being operated as slave controller.

3. The method according to claim **1** wherein said low-side controller circuit is being operated as slave controller and said high-side controller circuit is being operated as master controller.

4. The method according to claim **1** wherein to said main supply voltage terminal furnishing said main supply energy a direct current (DC) voltage source is connected.

5. The method according to claim **1** wherein to said main supply voltage terminal furnishing said main supply energy an alternating current (AC) voltage source is connected.

6. The method according to claim **1** wherein said low-side switching device and said high-side switching device are implemented as field effect transistors.

7. The method according to claim **6** wherein said field effect transistors are manufactured in NMOS-technology.

8. The method according to claim **6** wherein said field effect transistors are manufactured in PMOS-technology.

9. The method according to claim **1** wherein said low-side switching device and said high-side switching device are implemented as thyristors.

10. The method according to claim **9** wherein said thyristors are manufactured in bipolar-technology.

11. The method according to claim **9** wherein said thyristors are manufactured in MOS-technology, e.g. as GTO-thyristors (Gate Turn Off).

12. The method according to claim **1** wherein said low-side switching device and said high-side switching device are implemented as TRIACS (TRIode Alternating Current Switch).

13. The method according to claim **1** wherein said low-side switching device and said high-side switching device are implemented as DIACS (DIode Alternating Current Switch).

14. The method according to claim **1** wherein said low-side switching device and said high-side switching device are implemented as bipolar transistors.

15. The method according to claim **1** wherein said means for potential separation and isolation is implemented as an inductive signal transformer.

16. The method according to claim **1** wherein said means for potential separation and isolation is implemented as an optoelectric coupler or optoisolator.

17. The method according to claim **1** wherein said means for potential separation and isolation is implemented using differential capacitors.

18. The method according to claim **1** wherein said means for potential separation and isolation is implemented as a coupler, exploiting Giant Magnetoresistance (GMR) materials.

19. The method according to claim **1** wherein said step of starting-up an initial bootstrap procedure is implemented using a start-up voltage signal and a resistor.

20. A method for controlling and driving several higher voltage switching devices arranged within a circuit branch in serial connection and thus forming multiple output voltage terminals as mid-points between consecutive switching devices, all connected in series between a main supply voltage terminal furnishing the main supply energy and a ground terminal respectively, comprising:

providing said main supply voltage terminal, said output voltage terminal, said ground terminal, more than one of said external switching devices, an integrated master controller circuit, several integrated slave controller circuits and both types of circuits containing internal switches, means for generating, processing, and storing information data, means for transmitting/receiving said information data, means for transferring information; means for potential separation and isolation, storage means for said main supply energy, and several storage means for auxiliary supply energies;

arranging said several external switching devices in serial connection between said power terminal of the circuit, feeding input for the available main supply energy and said ground terminal;

associating to each of said external switching device its own appropriate controller circuit together with its own, individually controlled and regulated appliance for the required auxiliary energy supply;

assigning for said main supply energy and said different supply energies said separate and individual storage means;

transporting, controlling and regulating said energies with the help of said internal switches in said integrated master controller circuit and in said several integrated slave controller circuits;

generating, processing, and storing information data within said controller circuits for the purpose of control and regulation of each supply energy;

transferring and/or exchanging of said information data with a sufficiently isolating internal potential separation as means for transferring information within and between said controller circuits;

starting-up an initial bootstrap procedure for controlling and regulating said available main supply energy with said external switching devices together with generating said auxiliary supply energies, as needed for regular operation of said controller circuits;

generating, processing, and storing said information data within said controller circuits for the purpose of transportation as well as control and regulation of said every single supply energy, in order to solve the required control task;

setting-up and following a multi segment time slot scheme;

controlling and driving of said internal switching devices with the help of said controller circuits and said generated information data within the rules of said time slot scheme; and

transferring and/or exchanging of said information data by transmitting and receiving said information data with said means for transferring information between said controller circuits;

setting-up of the controlling and the driving of said external switching devices with the help of said information data using said controller circuits;

transporting and storing said energies between and in said storage devices with the help of said internal switches;

controlling and regulating said stored auxiliary supply energies according to the boundary conditions to be kept for the required control solution;

synchronizing all that within the framework of said time slot scheme; and at the same time

operating regularly in a closed loop of operations.

21. The method according to claim **20** wherein said integrated master controller circuit is located at the lowest possible position within said ladder structure i.e. closest to said ground terminal.

22. The method according to claim **20** wherein to said main supply voltage terminal furnishing said main supply energy a direct current (DC) voltage source is connected.

23. The method according to claim **20** wherein to said main supply voltage terminal furnishing said main supply energy an alternating current (AC) voltage source is connected.

24. The method according to claim **20** wherein said low-side switching device and said high-side switching device are implemented as field effect transistors.

25. The method according to claim **24** wherein said field effect transistors are manufactured in NMOS-technology.

26. The method according to claim **24** wherein said field effect transistors are manufactured in PMOS-technology.

27. The method according to claim **20** wherein said low-side switching device and said high-side switching device are implemented as thyristors.

28. The method according to claim **27** wherein said thyristors are manufactured in bipolar-technology.

29. The method according to claim **27** wherein said thyristors are manufactured in MOS-technology, e.g. as GTO-thyristors (Gate Turn Off).

30. The method according to claim **20** wherein said low-side switching device and said high-side switching device are implemented as TRIACS (TRIode Alternating Current Switch).

31. The method according to claim **20** wherein said low-side switching device and said high-side switching device are implemented as DIACS (DIode Alternating Current Switch).

32. The method according to claim **20** wherein said low-side switching device and said high-side switching device are implemented as bipolar transistors.

33. The method according to claim **20** wherein said means for potential separation and isolation is implemented as an inductive signal transformer.

34. The method according to claim **20** wherein said means for potential separation and isolation is implemented as an optoelectric coupler or optoisolator.

35. The method according to claim **20** wherein said means for potential separation and isolation is implemented using differential capacitors.

36. The method according to claim **20** wherein said means for potential separation and isolation is implemented as a coupler, exploiting Giant Magnetoresistance (GMR) materials.

37. The method according to claim **20** wherein said step of starting-up an initial bootstrap procedure is implemented using a start-up voltage signal and a resistor.

38. A circuit, capable of controlling and driving higher voltage switching devices, such as transistors, thyristors or triacs, which are configured as a half-bridge circuit branch, i.e. forming an output voltage terminal as mid-point between a high-side and a low-side switching device, both connected in series between a main supply voltage terminal - furnishing the main supply energy - and a ground terminal, further including low-side and high-side controller circuits having external terminals for signals and supply or start-up voltages and currents as well as a terminal for control data input and output,

comprising:

means for controlling and driving said low-side switching device, designated as integrated low-side controller circuit;

means for controlling and driving said high-side switching device, designated as integrated high-side controller circuit;

means for generating, storing, and processing information data, within said integrated low-side controller circuit and said integrated high-side controller circuit;

means for transmitting and/or receiving information data, within said integrated low-side controller circuit and said integrated high-side controller circuit;

means for transferring information data, between said integrated low-side controller circuit and said integrated high-side controller circuit;

means for potential separation and isolation of said means for transferring information between said integrated low-side controller circuit and said integrated high-side controller circuit;

means for storing said main supply energy, placed between and connected to said integrated low-side controller circuit and said integrated high-side controller circuit;

means for storing the low-side auxiliary supply energy for said integrated low-side controller circuit;

means for storing the high-side auxiliary supply energy for said integrated high-side controller circuit;

means for transporting said main supply energy into said means for storing said low-side auxiliary supply energy;

means for transporting said main supply energy into said means for storing said high-side auxiliary supply energy;

means for generating, controlling and regulating said low-side and said high-side auxiliary supply energies;

means for starting-up the operation of said means for generating, controlling and regulating said low-side and said high-side auxiliary supply energies during an initial bootstrapping procedure; and

means for generating and controlling said low-side and said high-side output signals driving said switching devices.

39. The circuit according to claim **38** wherein said integrated low-side controller circuit is being operated as master controller and said integrated high-side controller circuit is being operated as slave controller.

40. The circuit according to claim **38** wherein said integrated low-side controller circuit is being operated as slave controller and said integrated high-side controller circuit is being operated as master controller.

41. The circuit according to claim **38** wherein to said main supply voltage terminal furnishing said main supply energy a direct current (DC) voltage source is connected.

42. The circuit according to claim **38** wherein to said main supply voltage terminal furnishing said main supply energy an alternating current (AC) voltage source is connected.

43. The circuit according to claim **38** wherein said low-side switching device and said high-side switching device are implemented as field effect transistors.

44. The circuit according to claim **43** wherein said field effect transistors are manufactured in NMOS-technology.

45. The circuit according to claim **43** wherein said field effect transistors are manufactured in PMOS-technology.

46. The circuit according to claim **38** wherein said low-side switching device and said high-side switching device are implemented as thyristors.

47. The circuit according to claim **46** wherein said thyristors are manufactured in bipolar-technology.

48. The circuit according to claim **46** wherein said thyristors are manufactured in MOS-technology, e.g. as GTO-thyristors (Gate Turn Off).

49. The circuit according to claim **38** wherein said low-side switching device and said high-side switching device are implemented as TRIACS (TRIode Alternating Current Switch).

50. The circuit according to claim **38** wherein said low-side switching device and said high-side switching device are implemented as DIACS (DIode Alternating Current Switch).

51. The circuit according to claim **38** wherein said low-side switching device and said high-side switching device are implemented as bipolar transistors.

52. The circuit according to claim **38** wherein said means for potential separation and isolation is located internal to said integrated master controller circuit.

53. The circuit according to claim **38** wherein said means for potential separation and isolation is located internal to said integrated slave controller circuit.

54. The circuit according to claim **38** wherein said means for potential separation and isolation is located between said integrated master control circuit and said integrated slave controller circuit.

55. The circuit according to claim **38** wherein said means for potential separation and isolation is implemented as an inductive signal transformer.

56. The circuit according to claim **38** wherein said means for potential separation and isolation is implemented as an optoelectric coupler or optoisolator.

57. The circuit according to claim **38** wherein said means for potential separation and isolation is implemented using differential capacitors.

58. The circuit according to claim **38** wherein said means for potential separation and isolation is implemented as a coupler, exploiting Giant Magnetoresistance (GMR) materials.

59. The circuit according to claim **38** wherein said means for storing said main supply energy is implemented as a serial circuit of a generic resistive element with an energy storing capacitor.

60. The circuit according to claim **59** wherein said generic resistive element is specifically realized as a simple straight wire.

61. The circuit according to claim **59** wherein said generic resistive element is specifically realized as a resistor.

62. The circuit according to claim **59** wherein said generic resistive element is specifically realized as an inductor.

63. The circuit according to claim **38** wherein said means for storing the low-side auxiliary supply energy is realized with an energy storing capacitor.

64. The circuit according to claim **38** wherein said means for storing the high-side auxiliary supply energy is realized with an energy storing capacitor.

65. The circuit according to claim **38** wherein said means for storing the low-side auxiliary supply energy is realized with an energy storing capacitor.

66. The circuit according to claim **38** wherein said means for transporting said main supply energy into said means for storing said low-side auxiliary supply energy is implemented with integrated semiconductor switching devices.

67. The circuit according to claim **38** wherein said means for transporting said main supply energy into said means for storing said high-side auxiliary supply energy is implemented with integrated semiconductor switching devices.

68. The circuit according to claim **38** wherein said means for starting-up the operation during an initial bootstrap procedure is implemented using a start-up voltage signal and a resistor.

69. A circuit, capable of controlling and driving several higher voltage switching devices, such as transistors, thyristors or triacs, which are configured as a serial connection of said several switching devices, implementing a structure of switches comparable to the steps of a ladder, i.e. forming multiple output voltage terminals as mid-points between every two consecutive switching devices, all

together connected in series between a main supply voltage terminal - furnishing the main supply energy - and a ground terminal, further including a master and several slave controller circuits having external terminals for signals and supply or start-up voltages and currents as well as terminals for control data input and output,

comprising:

means for controlling and driving a first switching device, designated as integrated master controller circuit;

means for controlling and driving said switching devices other than said first switching device, designated as integrated slave controller circuits;

means for generating, storing, and processing information data, within said integrated master controller circuit and said integrated slave controller circuits;

means for transmitting and/or receiving information data, within said integrated master controller circuit and said integrated slave controller circuits;

means for transferring information data, between said integrated master controller circuit and said integrated slave controller circuits;

means for potential separation and isolation of said means for transferring information between said integrated master controller circuit and said integrated slave controller circuits;

means for storing said main supply energy, placed between and connected to said integrated master controller circuit and/or said integrated slave controller circuits;

means for storing the auxiliary supply energy for said integrated master controller circuit;

means for storing the auxiliary supply energies for said integrated slave controller circuits;

means for transporting said main supply energy into said means for storing said auxiliary supply energy for said integrated master controller circuit;

means for transporting said main supply energy into said means for storing said auxiliary supply energies for said integrated slave controller circuits;

means for generating, controlling and regulating said auxiliary supply energies;

means for starting-up the operation of said means for generating, controlling and regulating said auxiliary supply energies during an initial bootstrapping procedure; and

means for generating and controlling said output signals driving said several switching devices.

70. The circuit according to claim **69** wherein said integrated master controller circuit is located at the lowest possible position within said ladder structure i.e. closest to said ground terminal.

71. The circuit according to claim **69** wherein to said main supply voltage terminal furnishing said main supply energy a direct current (DC) voltage source is connected.

72. The circuit according to claim **69** wherein to said main supply voltage terminal furnishing said main supply energy an alternating current (AC) voltage source is connected.

73. The circuit according to claim **69** wherein said low-side switching device and said high-side switching device are implemented as field effect transistors.

74. The circuit according to claim **73** wherein said field effect transistors are manufactured in NMOS-technology.

75. The circuit according to claim **73** wherein said field effect transistors are manufactured in PMOS-technology.

76. The circuit according to claim **69** wherein said low-side switching device and said high-side switching device are implemented as thyristors.

77. The circuit according to claim **76** wherein said thyristors are manufactured in bipolar-technology.

78. The circuit according to claim **76** wherein said thyristors are manufactured in MOS-technology, e.g. as GTO-thyristors (Gate Turn Off).

79. The circuit according to claim **69** wherein said low-side switching device and said high-side switching device are implemented as TRIACS (TRIode Alternating Current Switch).

80. The circuit according to claim **69** wherein said low-side switching device and said high-side switching device are implemented as DIACS (DIode Alternating Current Switch).

81. The circuit according to claim **69** wherein said low-side switching device and said high-side switching device are implemented as bipolar transistors.

82. The circuit according to claim **69** wherein said means for potential separation and isolation is located internal to said integrated master controller circuit.

83. The circuit according to claim **69** wherein said means for potential separation and isolation is located internal to said integrated slave controller circuit.

84. The circuit according to claim **69** wherein said means for potential separation and isolation is located between said integrated master control circuit and said integrated slave controller circuit.

85. The circuit according to claim **69** wherein said means for potential separation and isolation is implemented as an inductive signal transformer.

86. The circuit according to claim **69** wherein said means for potential separation and isolation is implemented as an optoelectric coupler or optoisolator.

87. The circuit according to claim **69** wherein said means for potential separation and isolation is implemented using differential capacitors.

88. The circuit according to claim **69** wherein said means for potential separation and isolation is implemented as a coupler, exploiting Giant Magnetoresistance (GMR) materials.

89. The circuit according to claim **69** wherein said means for storing said main supply energy is implemented as a serial circuit of a generic resistive element with an energy storing capacitor.

90. The circuit according to claim **89** wherein said generic resistive element is specifically realized as a simple straight wire.

91. The circuit according to claim **89** wherein said generic resistive element is specifically realized as a resistor.

92. The circuit according to claim **89** wherein said generic resistive element is specifically realized as an inductor.

93. The circuit according to claim **69** wherein said means for storing the low-side auxiliary supply energy is realized with an energy storing capacitor.

94. The circuit according to claim **69** wherein said means for storing the high-side auxiliary supply energy is realized with an energy storing capacitor.

95. The circuit according to claim **69** wherein said means for storing the low-side auxiliary supply energy is realized with an energy storing capacitor.

96. The circuit according to claim **69** wherein said means for transporting said main supply energy into said means for storing said low-side auxiliary supply energy is implemented with integrated semiconductor switching devices.

97. The circuit according to claim **69** wherein said means for transporting said main supply energy into said means for storing said high-side auxiliary supply energy is implemented with integrated semiconductor switching devices.

98. The circuit according to claim **69** wherein said means for starting-up the operation during an initial bootstrap procedure is implemented using a start-up voltage signal and a resistor.

99. A circuit, capable of controlling and driving higher voltage switching devices, such as transistors, thyristors or triacs, which are configured as a half-bridge circuit branch, i.e. forming an output voltage terminal as mid-point between a

high-side and a low-side switching device, both connected in series between a main supply voltage terminal - furnishing the main supply energy - and a ground terminal, further including integrated low-side and high-side controller circuits having external terminals for signals and supply or start-up voltages and currents as well as a terminal for control data input and output, comprising:

said low-side switching device, one contact connected to said ground terminal and the other contact connected to said output voltage terminal and mid-point of said half-bridge;

said high-side switching device, one contact connected to said output voltage terminal and mid-point of said half-bridge and the other contact connected to said main supply voltage terminal;

said integrated low-side controller circuit for generating, storing, and processing information data as well as for controlling and driving said low-side switching device having an output signal terminal connected to the control input of said low-side switching device, further having two signal terminals for transmitting and/or receiving information data, having two terminals for said supply and start-up voltage, and having a terminal for said supply current;

said integrated high-side controller circuit for generating, storing, and processing information data as well as for controlling and driving said high-side switching device having an output signal terminal connected to the control input of said high-side switching device, further having two signal terminals for transmitting and/or receiving information data, having two terminals for said supply and start-up voltage, and having a terminal for said supply current;

a first capacitor for storing the low-side auxiliary supply energy for said integrated low-side controller circuit and connected with one point to said supply voltage terminal of said controller circuit and connected with the other point to said ground terminal;

a second capacitor for storing the high-side auxiliary supply energy for said integrated high-side controller circuit and connected with one point to said supply voltage terminal of said controller circuit and connected with the other point to said output voltage terminal at said mid-point of said half-bridge;

a combination of a capacitor - for storing the main supply energy – serially connected to a general resistive element, thus forming a two-pole circuit, placed between said integrated low-side controller circuit and said integrated high-side controller circuit and connected each with one of its two poles to said terminals for said supply current at each of said integrated controller circuits;

a two-wire connection between said integrated low-side controller circuit and said integrated high-side controller circuit for transferring information data between said controller circuits and each side of the wires connected to said signal terminals at each of said controller circuits;

a coupling element or four-pole circuit as device for potential separation and isolation of said two-wire connection between said integrated low-side controller circuit and said integrated high-side controller and connected to each of said signal terminals at each of said controller circuits;

a first pair of internal switching devices - internal to said integrated low-side controller circuit and conjointly connected each with one contact to said

terminal for said supply current - for transporting said main supply energy into said first capacitor for storing said low-side auxiliary supply energy, having the other contacts of said switching devices connected to said supply voltage terminal of said controller circuit and to said ground terminal respectively;

a second pair of internal switching devices - internal to said integrated high-side controller circuit and conjointly connected each with one contact to said terminal for said supply current - for transporting said main supply energy into said second capacitor for storing said high-side auxiliary supply energy, having the other contacts of said switching devices connected to said supply voltage terminal of said controller circuit and to said output voltage terminal at said mid-point of said half-bridge respectively;

internal circuit blocks within each of said integrated controller circuits for data processing, data storage and data driving for generating, controlling and regulating said low-side and said high-side auxiliary supply energies appropriately connected to each other and to said internal switching devices, having also connections to said signal and control terminals as well as to said supply voltage terminals, to said ground terminals or said output voltage terminals of said controller circuits;

two resistors for starting-up the operation of said internal circuit blocks for generating, controlling and regulating said low-side and said high-side auxiliary supply energies during an initial bootstrapping procedure and connected each with one point to an external start-up DC-voltage and each with its other point to said supply voltage terminals of each of said controller circuits; and

internal circuit blocks within each of said integrated controller circuits for data processing, data storage and data driving for generating and controlling said low-side and said high-side output signals driving said output terminals of said integrated controller circuits appropriately connected to each other and to said internal switching devices, having also connections to said signal and control terminals as well as to said supply voltage terminals, to said ground terminals or said output voltage terminals of said controller circuits.

100. The circuit according to claim **99** wherein to said main supply voltage terminal furnishing said main supply energy a direct current (DC) voltage source is connected.

101. The circuit according to claim **99** wherein to said main supply voltage terminal furnishing said main supply energy an alternating current (AC) voltage source is connected.

102. The circuit according to claim **99** wherein said integrated low-side controller circuit is being operated as master controller and said integrated high-side controller circuit is being operated as slave controller.

103. The circuit according to claim **99** wherein said integrated low-side controller circuit is being operated as slave controller and said integrated high-side controller circuit is being operated as master controller.

104. The circuit according to claim **102** wherein said master controller has a terminal for said control data input and output.

105. The circuit according to claim **103** wherein said master controller has a terminal for said control data input and output.

106. The circuit according to claim **99** wherein said low-side switching device and said high-side switching device are implemented as field effect transistors.

107. The circuit according to claim **106** wherein said field effect transistors are manufactured in NMOS-technology.

108. The circuit according to claim **106** wherein said field effect transistors are manufactured in PMOS-technology.

109. The circuit according to claim **99** wherein said low-side switching device and said high-side switching device are implemented as thyristors.

110. The circuit according to claim **109** wherein said thyristors are manufactured in bipolar-technology.

111. The circuit according to claim **109** wherein said thyristors are manufactured in MOS-technology, e.g. as GTO-thyristors (Gate Turn Off).

112. The circuit according to claim **99** wherein said low-side switching device and said high-side switching device are implemented as TRIACS (TRIode Alternating Current Switch).

113. The circuit according to claim **99** wherein said low-side switching device and said high-side switching device are implemented as DIACS (DIode Alternating Current Switch).

114. The circuit according to claim **99** wherein said low-side switching device and said high-side switching device are implemented as bipolar transistors.

115. The circuit according to claim **99** wherein said means for potential separation and isolation is located internal to said integrated master controller circuit.

116. The circuit according to claim **99** wherein said means for potential separation and isolation is located internal to said integrated slave controller circuit.

117. The circuit according to claim **99** wherein said means for potential separation and isolation is located between said integrated master control circuit and said integrated slave controller circuit.

118. The circuit according to claim **99** wherein said means for potential separation and isolation is implemented as an inductive signal transformer.

119. The circuit according to claim **99** wherein said means for potential separation and isolation is implemented as an optoelectric coupler or optoisolator.

120. The circuit according to claim **99** wherein said means for potential separation and isolation is implemented using differential capacitors.

121. The circuit according to claim **99** wherein said means for potential separation and isolation is implemented as a coupler, exploiting Giant Magnetoresistance (GMR) materials.

122. The circuit according to claim **99** wherein said means for storing said main supply energy is implemented as a serial circuit of a generic resistive element with an energy storing capacitor.

123. The circuit according to claim **122** wherein said generic resistive element is specifically realized as a simple straight wire.

124. The circuit according to claim **122** wherein said generic resistive element is specifically realized as a resistor.

125. The circuit according to claim **122** wherein said generic resistive element is specifically realized as an inductor.

126. The circuit according to claim **99** wherein said first pair of internal switching devices is implemented with integrated semiconductor switching devices.

127. The circuit according to claim **99** wherein said second pair of internal switching devices is implemented with integrated semiconductor switching devices.

128. The circuit according to claim **99** manufactured in monolithic integrated circuit technology.

129. The circuit according to claim **99** manufactured in monolithic integrated CMOS technology.

130. The circuit according to claim **99** manufactured in monolithic integrated CMOS circuit technology with additional discrete PMOS and/or NMOS transistors.

131. The circuit according to claim **99** manufactured in monolithic integrated CMOS circuit technology with additional discrete PMOS and/or NMOS transistors with extended drain technology.

132. The circuit according to claim **99** manufactured in monolithic integrated CMOS technology with additional PMOS and/or NMOS transistors with extended drain technology, assembled in Chip-On-Chip technology.